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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,987	11/30/2001	Feng Dai	CS00-197/199	3473

28112 7590 11/19/2003

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EXAMINER	
PERKINS, PAMELA E	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 11/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/002,987	DAI ET AL.	
	Examin r	Art Unit	
	Pamela E Perkins	2822	

-- Th MAILING DATE of this communication appears on the cover sheet with th correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-15 and 23-25* is/are allowed.

6)☒ Claim(s) *1-7 and 16-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This office action is in response to the filing of the amendment on 18 August 2003. Claims 1-25 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jang et al. (6,037,018) in view of Sahota (5,923,993).

Jang et al. disclose a method of forming shallow trench isolation regions where a oxide layer (20) is deposit on a semiconductor substrate (10); silicon nitride etch stop layer (24) in deposited using a chemical vapor process (CVD) on the oxide layer (20); etching a plurality of isolation trenches (28) through the silicon nitride etch stop layer (24) into the semiconductor substrate (10); forming a liner layer (36) in the isolation trenches (28); depositing an oxide layer (50) over the silicon nitride etch stop layer (24) and within the isolation trenches (24) using a high density plasma chemical vapor deposition (HDP-CVD); etching away the oxide layer (50) overlying the silicon nitride etch stop layer (24) and then removing the silicon nitride etch stop layer (24). Jang et al. further disclose the silicon nitride etch stop layer (24) having a thickness between 1000 and 2000

Angstroms (col. 4, line 48 thru col. 8, line 56). Jang et al. do not disclose narrow active areas and wide active areas of the semiconductor substrate are left between the isolation trenches.

Sahota discloses a method of forming shallow trench isolation regions where a silicon nitride etch stop layer (103) in deposited using a chemical vapor process (CVD) on to a semiconductor substrate (101); etching a plurality of isolation trenches (401) through the silicon nitride etch stop layer (103) into the semiconductor substrate (101, whereby narrow active areas and wide active areas of the semiconductor substrate (101) are left between the isolation trenches (401); depositing an oxide layer (1201) over the silicon nitride etch stop layer (103) and within the isolation trenches using a high density plasma chemical vapor deposition (HDP-CVD); etching away the oxide layer (1201) overlying the silicon nitride etch stop layer (103) and then removing the silicon nitride etch stop layer (103) (col. 3, lines 14-40).

Since Jang et al. and Sahota are both from the same field of endeavor, a method of forming shallow trench isolation regions, the purpose disclosed by Sahota would have been recognized in the pertinent art of Jang et al. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Jang et al. by narrow active areas and wide active areas of the semiconductor substrate are left between the isolation trenches as taught by Sahota to produce isolations regions usable for fabrication of microelectronic circuit devices (abstract).

Referring to claim 3, Jang et al. the silicon nitride etch stop layer of claim 1 wherein the silicon nitride etch stop layer may have a thickness between 1000 and 2000 Angstroms (col. 4, lines 32-35). It is noted that the specification contains no disclosure of either the critical nature of the claimed concentrations or any unexpected results arising there from. It would have been obvious to one of ordinary skill in the art to have the thickness of the silicon nitride etch stop layer to have a thickness between 1500 and 2500 Angstroms since it has been held that "In such an situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) See MPEP § 2144.05.

Claims 5, 6, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jang et al. in view of Sahota as applied to claims 1-4 and16-19 above, and further in view of Fu et al. (6,426,272).

Jang et al. disclose a method of forming shallow trench isolation regions where a oxide layer (20) is deposit on a semiconductor substrate (10); silicon nitride etch stop layer (24) in deposited using a chemical vapor process (CVD) on the oxide layer (20); etching a plurality of isolation trenches (28) through the silicon nitride etch stop layer (24) into the semiconductor substrate (10); forming a liner layer (36) in the isolation trenches (28); depositing an oxide layer (50) over the silicon nitride etch stop layer (24) and within the isolation trenches (24) using a high density plasma chemical vapor deposition (HDP-CVD); etching away the oxide layer (50) overlying the silicon nitride etch stop layer (24) and then

removing the silicon nitride etch stop layer (24). Jang et al. further disclose the silicon nitride etch stop layer (24) having a thickness between 1000 and 2000 Angstroms (col. 4, line 48 thru col. 8, line 56). Jang et al. do not disclose removing the silicon etch stop layer using a hot phosphoric acid (H_3PO_4) dip.

Fu et al. disclose a method of forming shallow trench isolation regions where a oxide layer (12) is deposit on a semiconductor substrate (10); silicon nitride etch stop layer (14) in deposited using a chemical vapor process (CVD) on the oxide layer (12); etching a plurality of isolation trenches (25) through the silicon nitride etch stop layer (14) into the semiconductor substrate (10); forming a liner layer (30) in the isolation trenches (25); depositing an oxide layer (40) over the silicon nitride etch stop layer (14) and within the isolation trenches (25) using a high density plasma chemical vapor deposition (HDP-CVD); etching away the oxide layer (40) overlying the silicon nitride etch stop layer (14) and then removing the silicon nitride etch stop layer (14) using a hot phosphoric acid (H_3PO_4) dip (col. 2, line 51 thru col. 3, line 50).

Since Jang et al. and Fu et al. are both from the same field of endeavor, a method of forming shallow trench isolation regions, the purpose disclosed by Fu et al. would have been recognized in the pertinent art of Jang et al. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Jang et al. by removing the silicon nitride etch stop layer using a hot phosphoric acid (H_3PO_4) dip as taught by Fu et al. to reduce defects (col. 1, lines 36-43).

Claims 7 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jang et al. in view of Sahota as applied to claims 1-4 and 16-19 above, and further in view of Hao et a. (6,403,483).

Jang et al. disclose a method of forming shallow trench isolation regions where a oxide layer (20) is deposit on a semiconductor substrate (10); silicon nitride etch stop layer (24) in deposited using a chemical vapor process (CVD) on the oxide layer (20); etching a plurality of isolation trenches (28) through the silicon nitride etch stop layer (24) into the semiconductor substrate (10); forming a liner layer (36) in the isolation trenches (28); depositing an oxide layer (50) over the silicon nitride etch stop layer (24) and within the isolation trenches (24) using a high density plasma chemical vapor deposition (HDP-CVD); etching away the oxide layer (50) overlying the silicon nitride etch stop layer (24) and then removing the silicon nitride etch stop layer (24). Jang et al. further disclose the silicon nitride etch stop layer (24) having a thickness between 1000 and 2000 Angstroms (col. 4, line 48 thru col. 8, line 56). Jang et al. do not disclose fabricating semiconductor device structures on the semiconductor substrate between the isolation trenches.

Hao et al. disclose a method of forming shallow trench isolation regions where an oxide layer (120) is formed on a semiconductor substrate (100), forming a silicon nitride etch stop layer (160) over the oxide layer (120), using a chemical vapor process (CVD); etching an isolation trench (220) through the silicon nitride etch stop layer (160) and the oxide layer (120) into the semiconductor substrate (100); lining the isolation trench with an oxide (300);

depositing an oxide layer (400) over the silicon nitride etch stop layer (160) and within the isolation trench (220) using a high density plasma (HDP); etching away the oxide layer (400) overlying the silicon nitride etch stop layer (160), then removing the silicon nitride etch stop layer (160) and further fabricating semiconductor device structures (710, 730) on the semiconductor substrate (100) between the isolation trench (220). Hao et al. further disclose the silicon nitride etch stop layer (160) having a thickness between 2000 and 4000 Angstroms (col. 3, lines 1-51).

Since Jang et al. and Hao et al. are both from the same field of endeavor, a method of forming shallow trench isolation regions, the purpose disclosed by Hao et al. would have been recognized in the pertinent art of Jang et al. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Jang et al. by fabricating semiconductor device structures on the semiconductor substrate between the isolation trenches as taught by Hao et al. to prevent gaps in the isolation structures (col. 2, lines 1 and 2).

Allowable Subject Matter

Claims 8-15 and 23-25 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: prior art does not anticipate, teach, or suggest a method of forming shallow trench isolation regions where a first silicon nitride etch stop layer in deposited using a chemical vapor process (CVD) on to a semiconductor

substrate; etching a plurality of isolation trenches through the first silicon nitride etch stop layer into the semiconductor substrate, whereby narrow active areas and wide active areas of the semiconductor substrate are left between the isolation trenches; depositing an oxide layer over the first silicon nitride etch stop layer and within the isolation trenches using a high density plasma chemical vapor deposition (HDP-CVD); depositing a second silicon nitride etch stop layer over the oxide layer, removing the second silicon nitride etch stop layer overlying the wide active areas, etching away the oxide layer overlying the first silicon nitride etch stop layer and the removing the first silicon nitride etch stop layer and the second silicon nitride etch stop layer with a hot phosphoric acid (H_3PO_4) dip.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lim et al. (6,403,484) disclose a first and second etch stop layers. However, Lim et al. is commonly assigned with the present invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E Perkins whose telephone number is (703) 605-4299. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

PEP

AMIR ZARABIAN
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